HAORAN JIN

Contact: allenjin@umich.edu ⋄ allenjin123.github.io

EDUCATION

University of Michigan Sep. 2023 - present
Ph.D in Computer Engineering | Computer Architecture & EDA
Advisor: Prof. Nathaniel Bleier & Previous Advisor: Prof. George Tzimpragos

Shanghai Jiao Tong University Sep. 2019 - Aug. 2023
B.Eng in Electrical and Computer Engineering

HONORS AND AWARDS

- 2020,2021,2022 National Encouragement Scholarship
- 2019,2020,2021,2022 John Wu & Jane Sun Sunshine Scholarship
- 2020,2021,2022 SJTU Undergraduate Excellence Scholarship

PUBLICATION

- Haoran Jin*, Jirong Yang*, Barry Lyu, Ruijie Gao, Nathaniel Bleier, *æSIP: μArch-aware ASIP-ISA Co-Design via Program Synthesis, Equality Saturation, and External Don't Cares*, ISCA 2026 (Under Review)
- Haoran Jin, Jirong Yang, Alexia Moreno, Ruijie Gao, Barry Lyu, Nathaniel Bleier, *Scalable Hardware Pruning through Semiformal Verification and Microarchitecture Awareness*, DAC 2026 (Under Review)
- Haoran Jin, Jirong Yang, Yunpeng Liu, Barry Lyu, Kangqi Zhang, Nathaniel Bleier, *Mozart: An Ecosystem-Accelerator Codesign Framework for Composable, Heterogeneous Chiplet-based Neural Network Accelerators*, ASPLOS 2026 (Under Review)
- Zexi Li*, Haoran Jin*, Kuncai Zhong, Guojie Luo, Runsheng Wang, Weikang Qian, *SCGen: A Versatile Generator Framework for Agile Development of Stochastic Circuits*, DATE 2024
- Kuncai Zhong, Zexi Li, Haoran Jin, Weikang Qian, *Exploiting Uniform Spatial Distribution to Design Efficient Random Number Source for Stochastic Computing*, ICCAD 2022

SELECTED PROJECTS

æSIP: Arch-aware ASIP-ISA Co-Design via Program Synthesis, Equality Saturation, and External Don't Cares
Prof. Nathaniel Bleier at University of Michigan July. 2025 – Nov. 2025

- A program may use only a small subset of instructions from an ISA, making it possible to design ASIP by removing unused hardware without affecting correctness of programs.
- Proposed æSIP, a μArch-aware ASIP-ISA co-design framework that leverages hardware aware program rewriting to automatically generate an optimized ASIP-program pair.
- Built a program synthesis framework that leverages neuro-symbolic approach to automatically discover correctness-preserving rewrites that maximize hardware removal opportunities.

Mozart: An Ecosystem-Accelerator Codesign Framework for Composable, Heterogeneous Chiplet-based Neural Network Accelerators
Prof. Nathaniel Bleier at University of Michigan Jan. 2025 – Aug. 2025

- Developed a chiplet ecosystem-accelerator codesign framework to increase chiplet reuse and hence reducing non-recurring engineering costs.

- Built hierarchical design space exploration methodology to systematically compose heterogeneous chiplet-based bespoke ASIC leveraging operator-level disaggregation insights.
- Implemented constraint-aware optimization for datacenter LLM serving and autonomous vehicle case studies.

Minimum Area Retiming for xSFQ logic
Prof. George Tzimpragos at University of Michigan Aug. 2024 – Dec. 2024

- Developed a linear programming formulation to simultaneously minimize the number of registers and duplication logic in xSFQ circuits for optimal area reduction while maintaining clock period constraints.

Mixed Circuit of Binary & Stochastic Computing
Prof. Weikang Qian at SJTU Jan. 2022 – Sep. 2023

- Defined a domain-specific language (DSL) for agile mixed circuit development.
- Implemented a Verilog code generation backend for the DSL to facilitate hardware synthesis.
- Evaluated mixed binary-stochastic circuits for image processing applications.

SKILL

Programing	C, C++, Java, Python, Rust, Verilog HDL, SQL, LLVM IR, ELM
Tools	PyTorch, MatLab, Mathematica, Vitis HLS, Spark, Drill, Hadoop, Pin, Proteus, Pspice